IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/602,292	§	Examiner: Lai, Vincent
Filed: June 24, 2003	§	Group/Art Unit: 2181
Inventors:	§	Atty. Dkt. No: 5860-00101
Michael B. Doerr, William H. Hallidy, David A. Gibson and Craig M. Chase	§	
Title: PROCESSING SYSTEM WITH INTERSPERSED PROCESSORS AND COMMUNICATION ELEMENTS	§	

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir or Madam:

Applicants request review of the final rejection of June 2, 2006 in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal. The review is requested for the reason(s) stated below.

Claims 1-64 remain pending in the application. Reconsideration of the present case is earnestly requested in light of the following remarks. Please note that for brevity, only the primary arguments directed to the independent claims are presented, and that additional arguments, e.g., directed to the subject matter of the dependent claims, will be presented if and when the case proceeds to Appeal.

Claims 1-64 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Wilkinson et al. (U.S. Patent No. 5,805,915) (hereinafter, "Wilkinson"). Applicants traverse this rejection. The following clear errors in the Examiner's rejection are noted.

Contrary to the Examiner's assertion, Wilkinson fails to teach or suggest all of the limitations of claim 1, including a plurality of dynamically configurable communication elements and a plurality of dynamically configurable communication elements, each having specifically recited features, coupled together in an interspersed arrangement. As shown in Figures 2 and 4, Wilkinson teaches only a uniform array of interconnected picket processors 100, not an interspersed array of processors and communication

elements as recited in claim 1. The Examiner relies on Wilkinson, col. 23, lines 11-16 in asserting that DCC elements are "part of the picket array" of Wilkinson, pointing to col. 22, lines 30-67 in asserting that Wilkinson discloses the communication ports and memory features of the DCC elements of claim 1. Essentially, the Examiner is attempting to argue that each picket 100 of Wilkinson corresponds to both a processor and a communication element of claim 1. However, this interpretation renders the remainder of claim 1 incoherent, in that claim 1 requires that DCC elements have a first subset of communication ports configured for coupling to processors and a second subset of communication ports configured for coupling to other DCC elements. In attempting to show that Wilkinson satisfies this arrangement of connectivity, the Examiner refers to I/O ports 520 discussed at col. 22, lines 30-56 and col. 23, lines 1-16. However, I/O ports 520 have nothing to do with interfacing individual pickets 100 with one another. Rather, Wilkinson clearly discloses that these ports are configured for "communication to associated mainframes or otherwise to the rest of the world," (col. 22, lines 55-56) that is, for communication not among, but external to pickets 100.

Claim 1 requires that a processor including an ALU and an instruction processing unit be configured for coupling, via processor ports, to a subset of DCC elements each including a memory and a routing engine, where DCC elements in turn include ports configured for coupling to processors and other DCC elements. By contrast, Wilkinson discloses a plurality of pickets 100, each including its own memory 102, and each passively connected to one another via propagate and broadcast buses (as shown in Figure 2). Further, while claim 1 clearly requires that DCC elements include a routing engine, it is not clear from the disclosure of Wilkinson that any routing of communications is performed by the pickets themselves. Rather, Wilkinson clearly discloses that execution control of and communication among pickets 100 is controlled by instruction sequencer 402 and execution control 403, which are entirely distinct from and not interspersed among pickets 100 (Figure 4 and col. 20, lines 4-30).

In the "Response to Arguments" section of the Final Action, the Examiner asserts that "[n]owhere in Wilkinson is the array described as uniform," "Figures 2 and 4 are not enough evidence to prove uniformity," and "applicant did not clearly define the term interspersed and thus the broadest interpretation of the term (to place at intervals) was used." Applicants traverse these remarks and refer to Applicants' arguments in response to the Final Action (response mailed July 31, 2006) describing ample evidence for the uniformity of Wilkinson's array. Applicants note that claim 1 does not merely recite "an interspersed array." Rather, claim 1 recites that a plurality of processors and a plurality of dynamically configurable communication elements are coupled together in an interspersed arrangement. Wilkinson discloses a completely different system topology in which pickets are coupled together in a regular array.

Wilkinson fails to disclose any sort of element resembling Applicants' recited dynamically configurable communication element that is interspersed among the pickets as required by claim 1. In fact, as shown in Figures 2 and 4, Wilkinson discloses identically-configured pickets 100 directly coupled to one another.

Applicants further note that claim 1 does not merely recite communication elements, but rather communication elements distinct from and coupled together with processing elements in an interspersed arrangement. Merely identifying a feature in Wilkinson that could potentially be used for communication, as the Examiner has done, does not satisfy all of the limitations of the communication element as recited in claim 1. Moreover, merely inferring that communication among pickets requires some sort of port does not amount in any way to a disclosure of how those ports are configured for coupling to subsets of both the recited processors and other ones of the recited communication elements as recited in claim 1. The fact that Wilkinson does not disclose the basic configuration of elements required by claim 1 renders it impossible for Wilkinson to disclose the specific, claimed manner in which those elements are interconnected, as required for anticipation.

In the "Response to Arguments" section of the Final Action, the Examiner acknowledges that Wilkinson does not explicitly teach a routing engine, but asserts that because Wilkinson discusses routing in general, a routing engine is necessarily implied. Applicants note that the mere inference of a feature resembling a claimed element does not amount to a complete disclosure of the element as claimed. Notwithstanding the fact that Wilkinson fails to teach this element as fully required by claim 1, Wilkinson fails to ascribe routing functionality to any element actually within the picket array, instead providing a control bus to pickets 100 from execution control 403 residing external to the picket array (Figure 4 and col. 20, lines 4-24).

In addition to distinctions noted above for claim 1, Wilkinson fails to teach or suggest the limitation of claim 41 in which a stalling processor or DCC element is operable to propagate stalling information through one or more of intermediate subset of DCC elements to a source processor that is operable to suspend transfer of the first plurality of data upon receipt of the stalling information. The Examiner relies upon col. 19, lines 10-20 of Wilkinson to demonstrate that Wilkinson discloses the stalling behavior recited in claim 41. However, the cited portion of Wilkinson has nothing whatsoever to do with detecting or propagating stall behavior information, or responding to such information in any way. The cited portion refers to a particular example application of Wilkinson's system in which each picket 100 is assigned to model a particular gate or logic function of a digital system (col. 18, lines 62-

65). In particular, Wilkinson discloses broadcasting a name and value of a modeled signal to all pickets 100 in response to the modeled signal changing value, whereupon pickets 100 assigned to model gates having input signal names that match the broadcast name receive the changed value and accordingly modify the computed values of the gates (col. 19, lines 1-14). However, the broadcast information is not stalling information; in fact, it does not indicate anything about the operational status of a processor or DCC element at all. Rather, it is information indicative of the value of a logic signal modeled by a picket. Further, upon receipt of a broadcast signal name, Wilkinson does not suspend transfer of data. Rather, Wilkinson uses the receipt of a signal name as a trigger to capture the value associated with the signal name.

In the Advisory Action of August 15, 2006, the Examiner asserts that "A stall must be used in order to ensure that no more signal changes occur. Until signal changes stop, the parallel processes cannot continue and thus a stall must be necessary." Applicants traverse these statements and note that Wilkinson makes no such teaching, and that a stall is in no way necessary in Wilkinson's application as the Examiner suggests. Wilkinson specifically provides that the broadcast of signal names occurs "until no more signal changes occur or the process is stopped." (col. 19, lines 19-20) That is, Wilkinson describes a modeling system that runs continuously until quiescence occurs or is otherwise interrupted. Applicants reiterate that nothing in this brief discussion of an application of Wilkinson's system has anything to do with stalling behavior in a hardware system as recited in Applicants' claim 41.

Arguments given above also pertain to the remaining independent claims to the extent they recite similar features to claims 1 and 41. Applicants refer to the previous response to the Final Action for further detailed arguments with respect to other limitations of the remaining independent claims. For at least the foregoing reasons, Applicants submit that the Examiner's rejection of claims 1-64 is in error, and that these claims are clearly distinguishable over the cited art.

In light of the foregoing remarks, Applicants submit the application is in condition for allowance, and prompt notice to that effect is respectfully requested. If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above referenced application from becoming abandoned, Applicant hereby petitions for such an extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 501505/5860-00101/JCH.

Also filed herewith are the following item(s):

☒ Notice of Appeal

Respectfully submitted,

/Jeffrey C. Hood/

Jeffrey C. Hood, Reg. #35198
ATTORNEY FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800

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